

SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

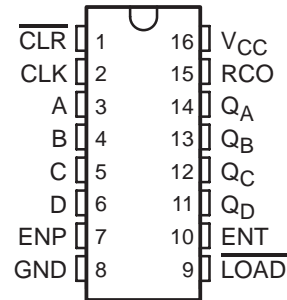
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

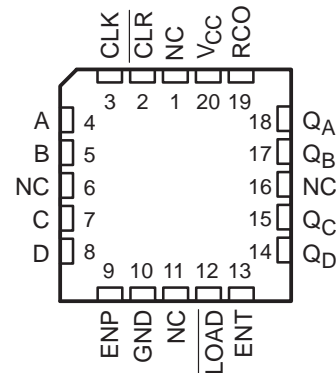
description/ordering information

The 'LV161A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

SN54LV161A . . . J OR W PACKAGE
SN74LV161A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV161A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 40	SN74LV161AD	LV161A
		Reel of 2500	SN74LV161ADR	
	SOP – NS	Reel of 2000	SN74LV161ANSR	74LV161A
	SSOP – DB	Reel of 2000	SN74LV161ADBR	LV161A
	TSSOP – PW	Tube of 90	SN74LV161APW	LV161A
		Reel of 2000	SN74LV161APWR	
Reel of 250		SN74LV161APWT		
TVSOP – DGV	Reel of 2000	SN74LV161ADGVR	LV161A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV161AJ	SNJ54LV161AJ
	CFP – W	Tube of 150	SNJ54LV161AW	SNJ54LV161AW
	LCCC – FK	Tube of 55	SNJ54LV161AFK	SNJ54LV161AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
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SN54LV161A, SN74LV161A

4-BIT SYNCHRONOUS BINARY COUNTERS

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description/ordering information (continued)

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'LV161A devices is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{\text{LOAD}}$), or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

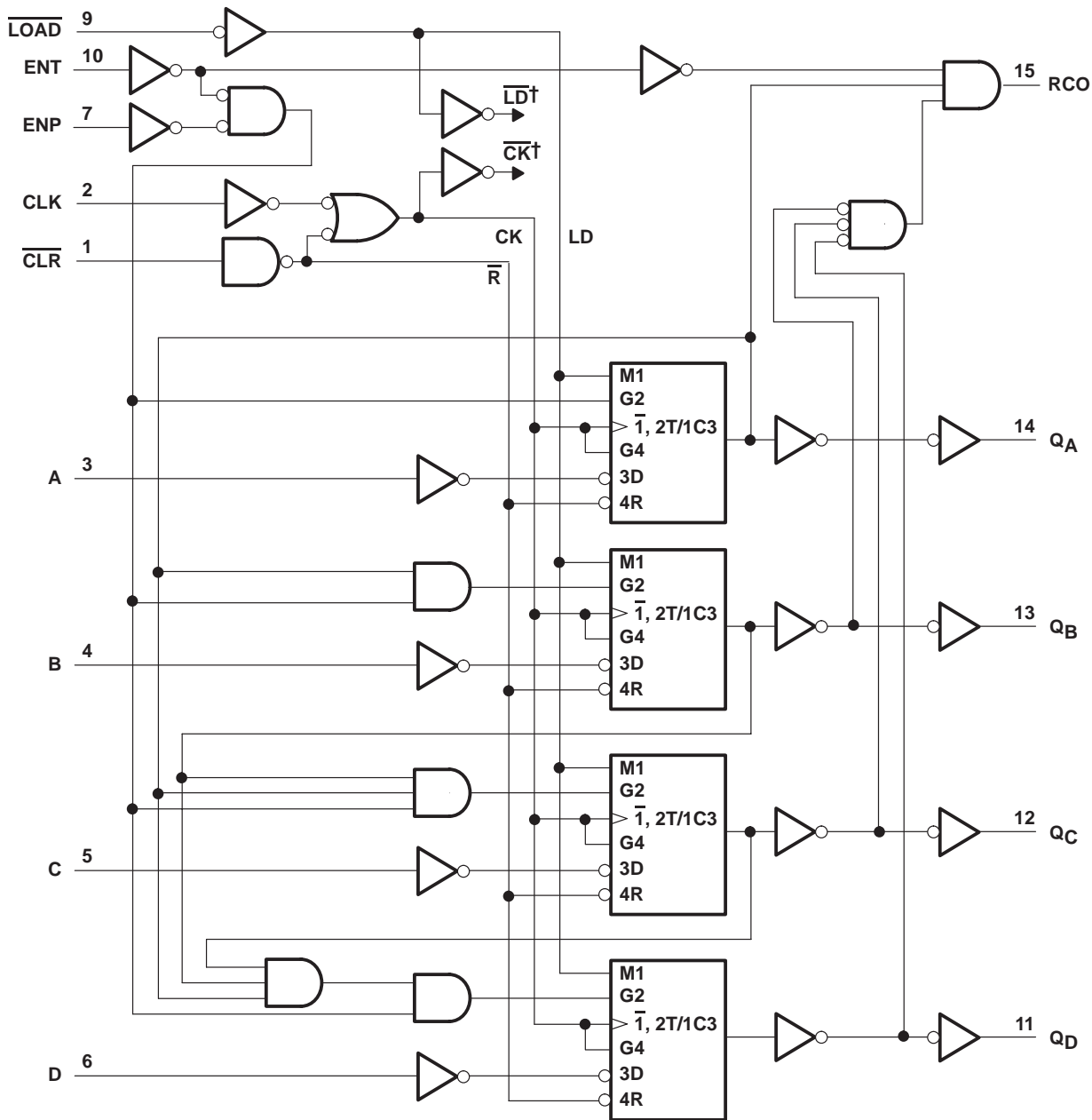
INPUTS					OUTPUTS				FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	ENP	ENT	CLK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	↑	No Change				No Count
H	H	L	X	↑	No Change				No Count
H	H	H	H	↑	Count up				Count
H	X	X	X	↑	No Change				No Count



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logic diagram (positive logic)



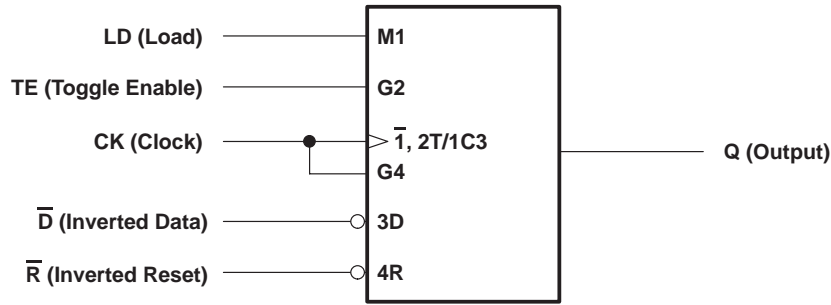
† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

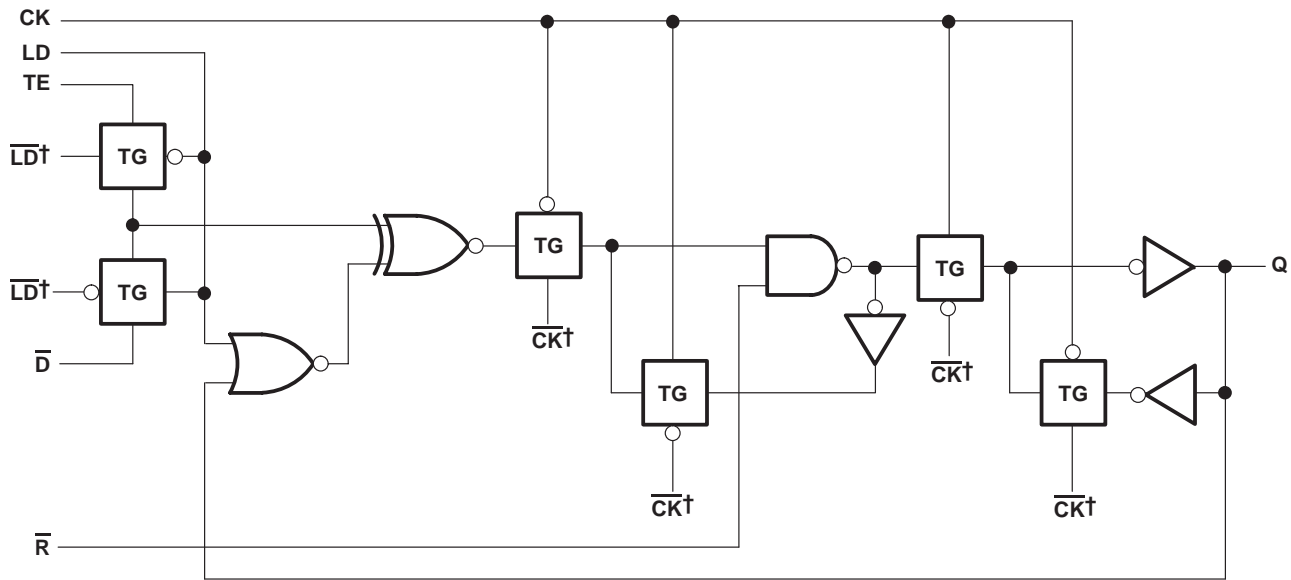
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logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

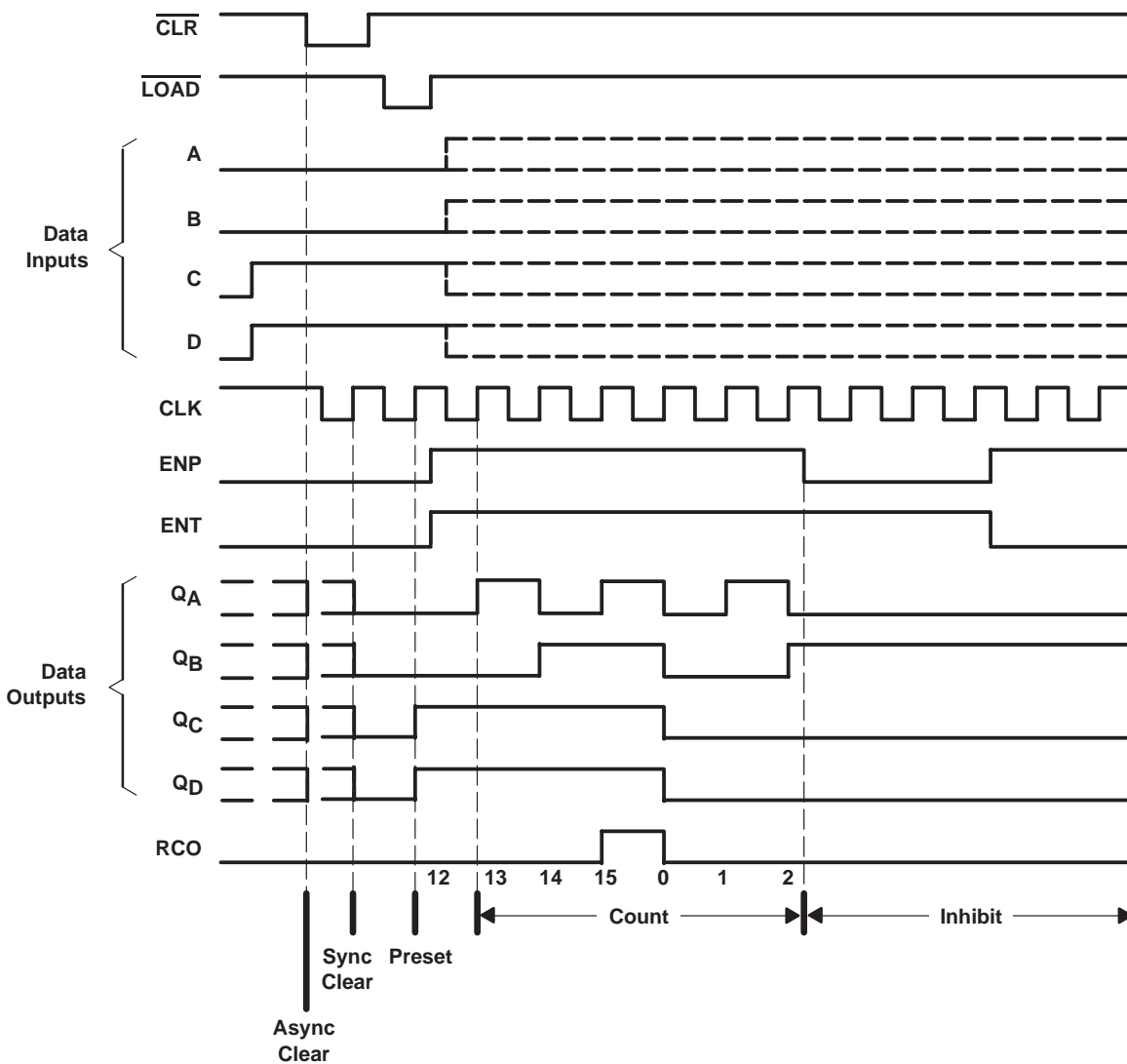


† The origins of \overline{LD} and \overline{CK} are shown in the overall logic diagram of the device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range applied in high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the power-off state, V_O (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

		SN54LV161A		SN74LV161A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	2	5.5	2	5.5	V	
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3			
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA	
		V _{CC} = 2.3 V to 2.7 V		-2	-2	mA	
		V _{CC} = 3 V to 3.6 V		-6	-6		
		V _{CC} = 4.5 V to 5.5 V		-12	-12		
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA	
		V _{CC} = 2.3 V to 2.7 V		2	2	mA	
		V _{CC} = 3 V to 3.6 V		6	6		
		V _{CC} = 4.5 V to 5.5 V		12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV161A			SN74LV161A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1		V	
	I _{OH} = -2 mA	2.3 V	2		2				
	I _{OH} = -6 mA	3 V	2.48		2.48				
	I _{OH} = -12 mA	4.5 V	3.8		3.8				
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V				0.1	0.1	V	
	I _{OL} = 2 mA	2.3 V				0.4	0.4		
	I _{OL} = 6 mA	3 V				0.44	0.44		
	I _{OL} = 12 mA	4.5 V				0.55	0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V				±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				20	20	μA	
I _{off}	V _I or V _O = 0 to 5.5 V	0				5	5	μA	
C _i	V _I = V _{CC} or GND	3.3 V		1.8		1.8		pF	

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7	7	7	7	ns	
		$\overline{\text{CLR}}$ low	7	7	7	7		
t_{su}	Setup time before CLK \uparrow	$\overline{\text{CLR}}$	4.5	4.5	4.5	ns		
		Data (A, B, C, and D)	7.5	8.5	8.5			
		ENP, ENT	9.5	11	11			
		$\overline{\text{LOAD}}$ low	10	11.5	11.5			
t_h	Hold time, all synchronous inputs after CLK \uparrow	1.5	1.5	1.5	1.5	ns		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5	5	5	ns		
		$\overline{\text{CLR}}$ low	5	5	5			
t_{su}	Setup time before CLK \uparrow	$\overline{\text{CLR}}$	2.5	2.5	2.5	ns		
		Data (A, B, C, and D)	5.5	6.5	6.5			
		ENP, ENT	7.5	9	9			
		$\overline{\text{LOAD}}$ low	8	9.5	9.5			
t_h	Hold time, all synchronous inputs after CLK \uparrow	1	1	1	1	ns		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV161A		SN74LV161A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5	5	5	ns		
		$\overline{\text{CLR}}$ low	5	5	5			
t_{su}	Setup time before CLK \uparrow	$\overline{\text{CLR}}$	1.5	1.5	1.5	ns		
		Data (A, B, C, and D)	4.5	4.5	4.5			
		ENP, ENT	5	6	6			
		$\overline{\text{LOAD}}$ low	5	6	6			
t_h	Hold time, all synchronous inputs after CLK \uparrow	1	1	1	1	ns		

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SN54LV161A, SN74LV161A 4-BIT SYNCHRONOUS BINARY COUNTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 V \pm 0.2 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15 \text{ pF}$	50*	125*		40*		40		MHz
			$C_L = 50 \text{ pF}$	30	95		25		25		
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$	7.9*	16.2*		1*	19.5*	1	19.5	ns
		RCO (count mode)		8.9*	17*		1*	20.5*	1	20.5	
		RCO (preset mode)		11.9*	20.6*		1*	24.5*	1	24.5	
	ENT	8.3*		15.7*		1*	19*	1	19		
t_{PHL}	$\overline{\text{CLR}}$	Q		8.8*	17*		1*	20.5*	1	20.5	
		RCO		9.8*	16.6*		1*	20*	1	20	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	10.5	19.2		1	22.5	1	22.5	ns
		RCO (count mode)		11.7	20		1	23.5	1	23.5	
		RCO (preset mode)		14.5	23.6		1	27.5	1	27.5	
	ENT	11		18.7		1	22	1	22		
t_{PHL}	$\overline{\text{CLR}}$	Q		11.4	20		1	23.5	1	23.5	
		RCO		12.6	19.6		1	23	1	23	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	80*	165*		70*	70		MHz	
			$C_L = 50 \text{ pF}$	55	125		50	50			
t_{pd}^*	CLK	Q	$C_L = 15 \text{ pF}$	6	12.8		1*	15*	1	15	ns
		RCO (count mode)		6.7	13.6		1*	16*	1	16	
		RCO (preset mode)		8.6	17.2		1*	20*	1	20	
	ENT	RCO		6.2	12.3		1*	14.5*	1	14.5	
t_{PHL}^*	\overline{CLR}	Q		6.5	13.6		1*	16*	1	16	
		RCO		7.2	13.2		1*	15.5*	1	15.5	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	7.8	16.3		1	18.5	1	18.5	ns
		RCO (count mode)		8.7	17.1		1	19.5	1	19.5	
		RCO (preset mode)		10.6	20.7		1	23.5	1	23.5	
	ENT	RCO		8.3	15.8		1	18	1	18	
t_{PHL}	\overline{CLR}	Q		8.4	17.1		1	19.5	1	19.5	
		RCO		9.2	16.7		1	19	1	19	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV161A		SN74LV161A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	135*	220		115*		115		MHz
			$C_L = 50\text{ pF}$	95	165		85		85		
t_{pd}	CLK	Q	$C_L = 15\text{ pF}$	4.5*	8.1*	1*	9.5*	1	9.5	ns	
		RCO (count mode)		5.1*	8.1*	1*	9.5*	1	9.5		
		RCO (preset mode)		6.3*	10.3*	1*	12*	1	12		
	ENT	4.8*		8.1*	1*	9.5*	1	9.5			
t_{PHL}	$\overline{\text{CLR}}$	Q		4.9*	9*	1*	10.5*	1	10.5		
		RCO		5.5*	8.6*	1*	10*	1	10		
t_{pd}	CLK	Q	$C_L = 50\text{ pF}$	5.9	10.1	1	11.5	1	11.5	ns	
		RCO (count mode)		6.6	10.1	1	11.5	1	11.5		
		RCO (preset mode)		7.8	12.3	1	14	1	14		
	ENT	6.1		10.1	1	11.5	1	11.5			
t_{PHL}	$\overline{\text{CLR}}$	Q		6.3	11	1	12.5	1	12.5		
		RCO		6.9	10.6	1	12	1	12		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV161A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.2	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	23.6	pF
			5 V	25.8	

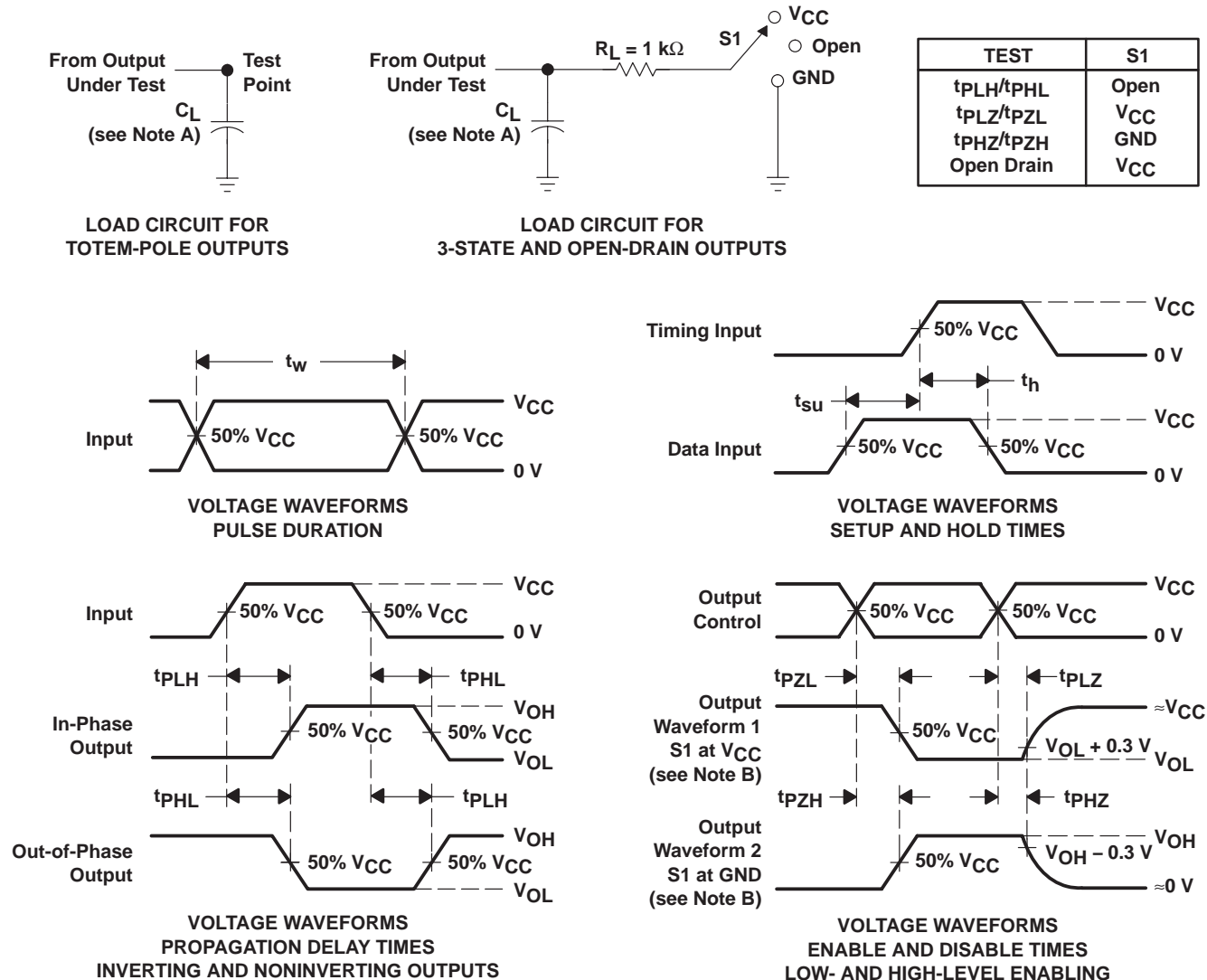
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV161AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV161APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

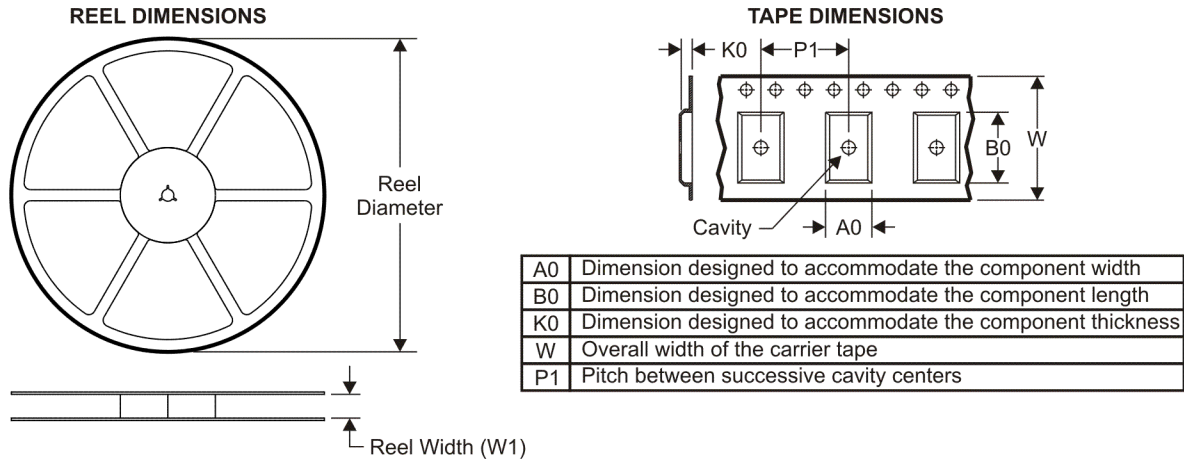
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV161ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV161ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV161ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV161APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV161APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV161ADBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74LV161ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74LV161ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV161ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LV161APWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN74LV161APWT	TSSOP	PW	16	250	346.0	346.0	29.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

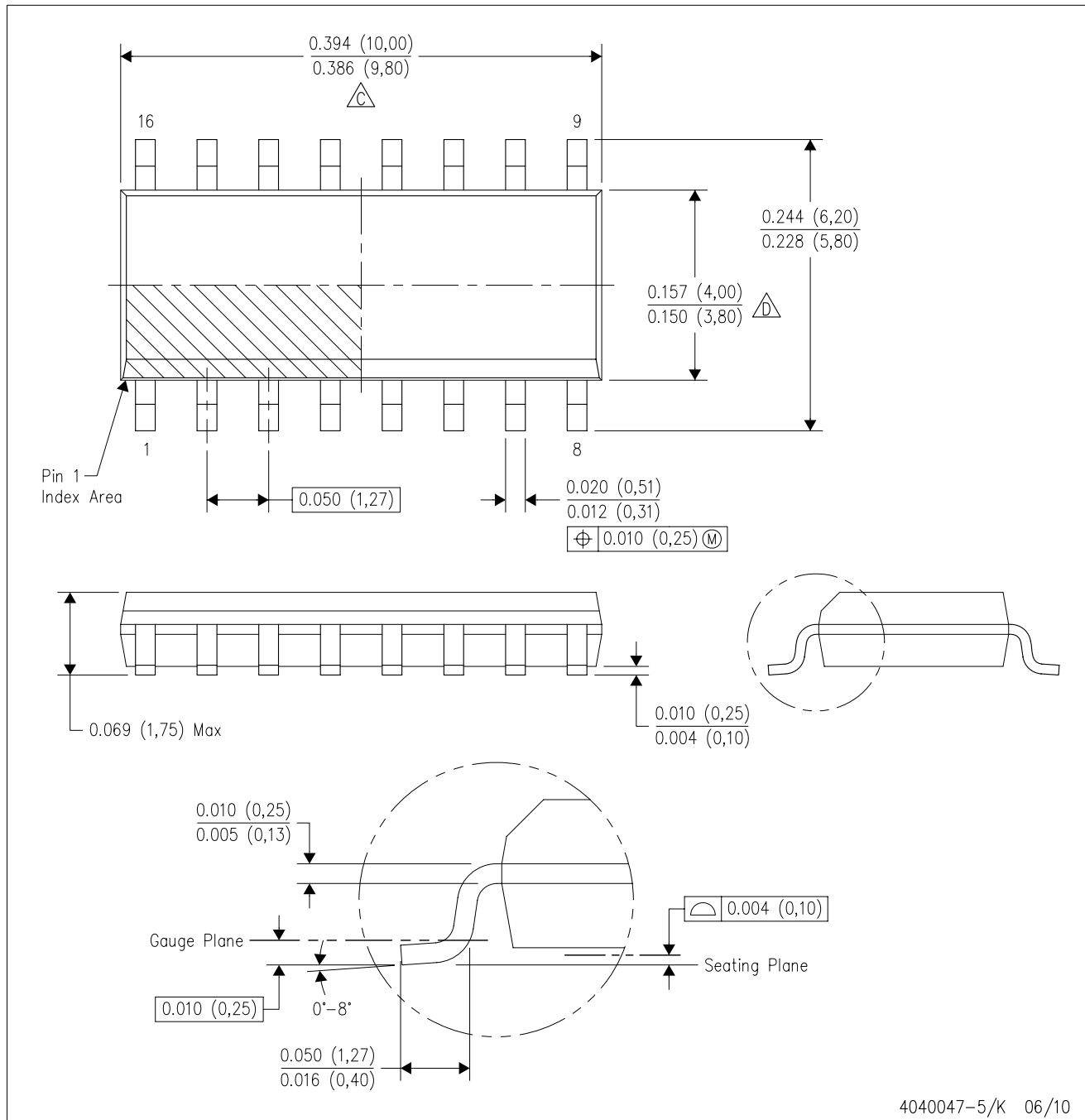
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

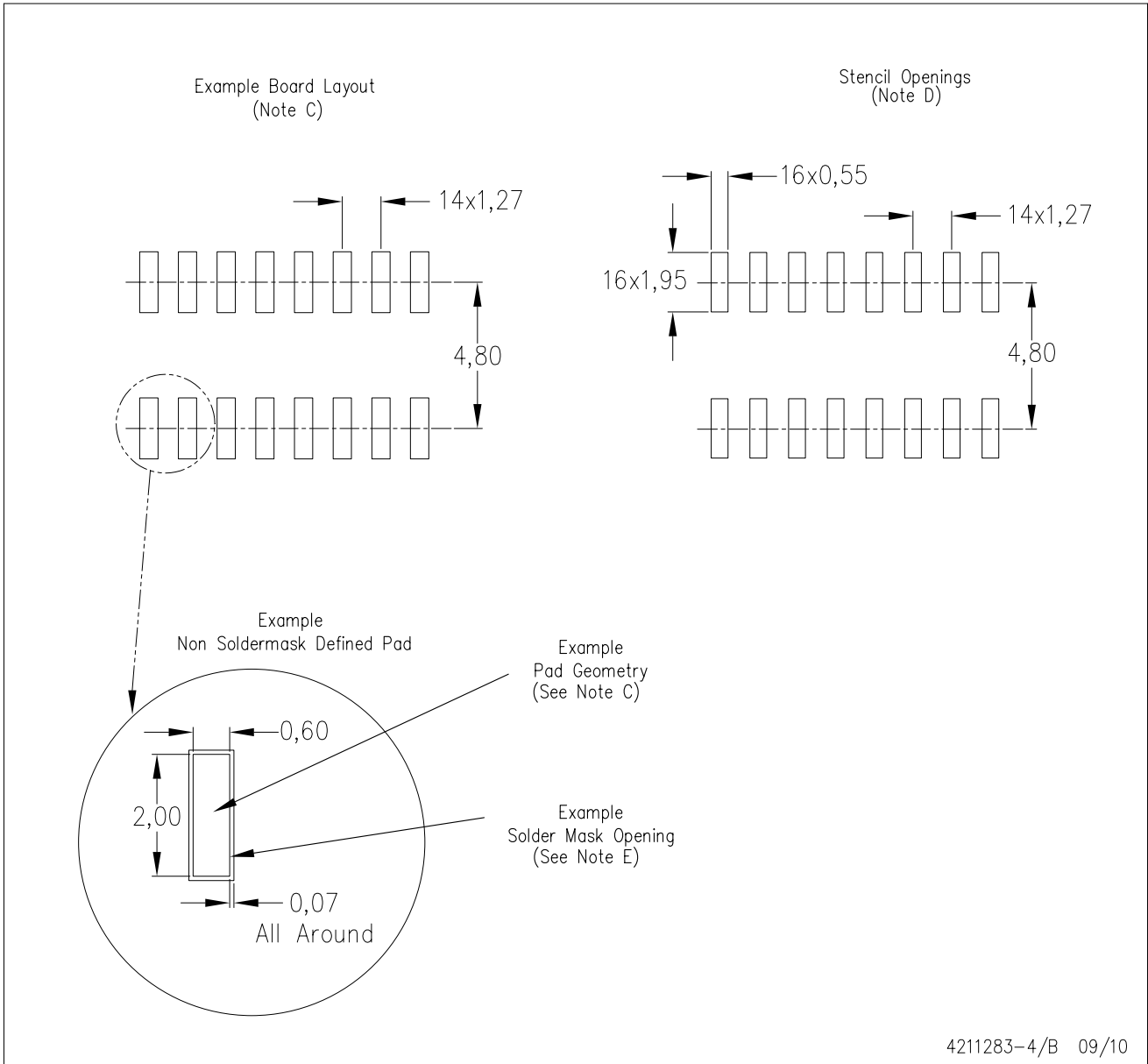
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

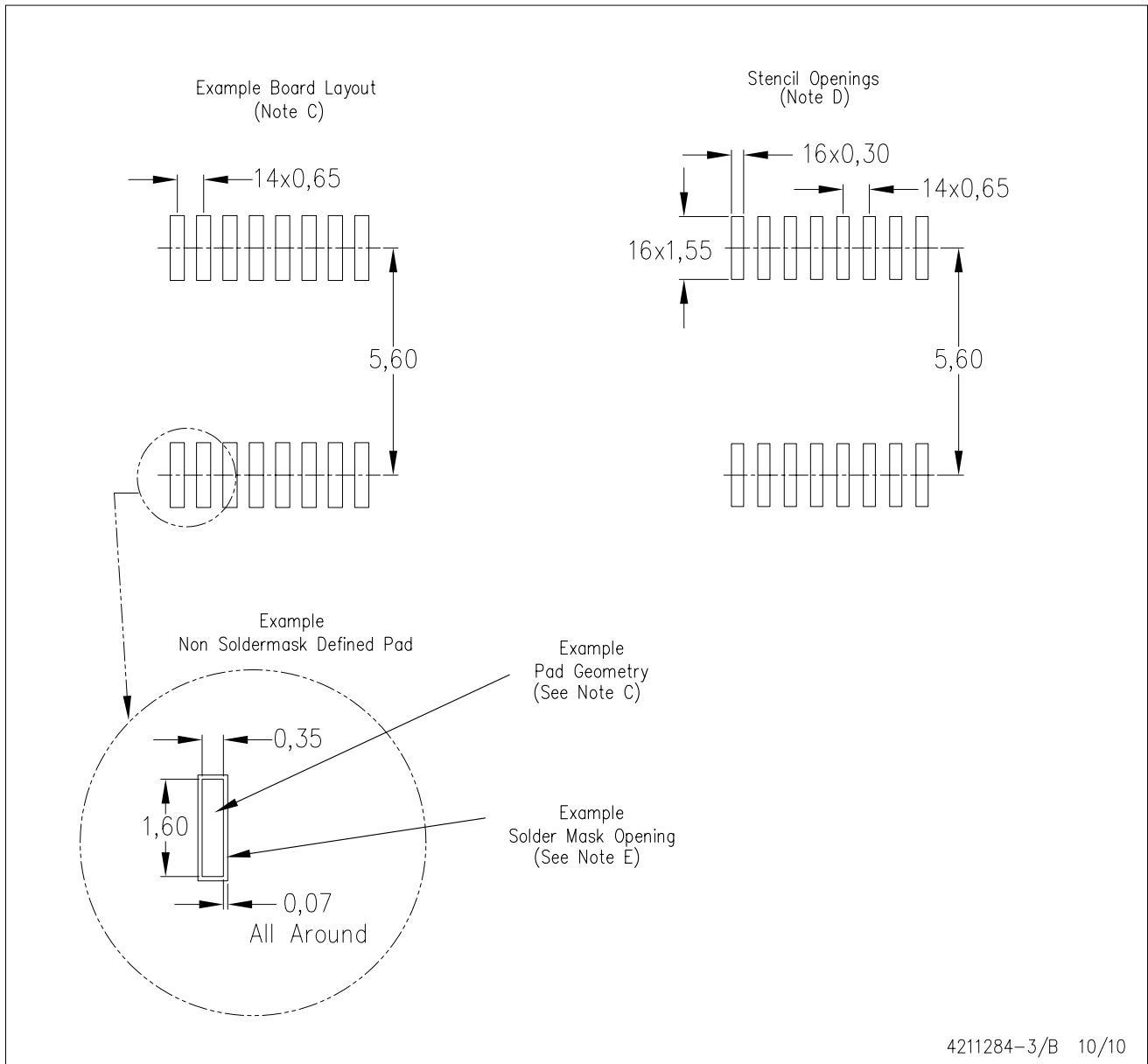


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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