

SN74LS19A, SN74LS24A SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

JANUARY 1981 — REVISED MARCH 1988

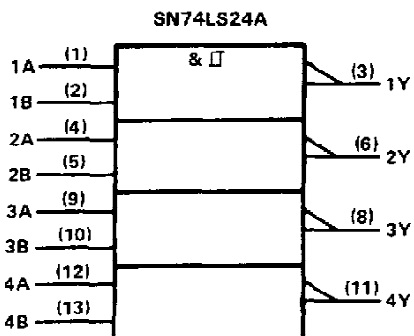
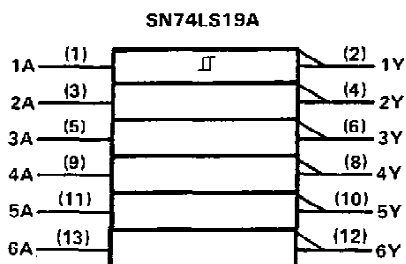
- Functionally and Mechanically Identical to 'LS13, 'LS14, and 'LS132, Respectively
- Improved Line-Receiving Characteristics
- P-N-P Inputs Reduce System Loading
- Excellent Noise Immunity with Typical Hysteresis of 0.8 V

description

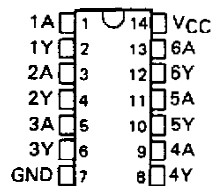
Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals. The hysteresis or backlash, which is the difference between the two threshold levels ($V_{T+} - V_{T-}$), is typically 800 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

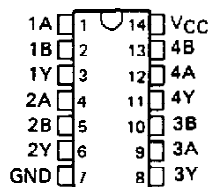
logic symbols †



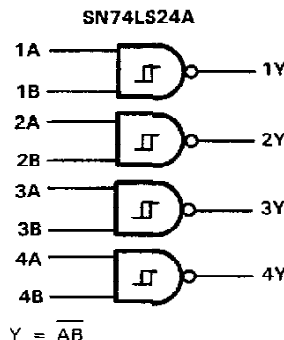
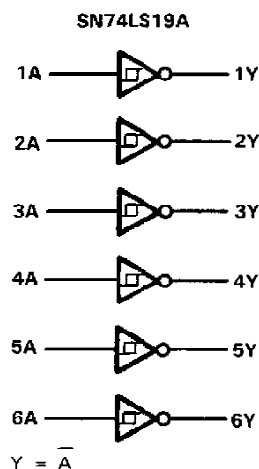
SN74LS19A . . . D, J, OR N PACKAGE
(TOP VIEW)



SN74LS24A . . . D, J, OR N PACKAGE
(TOP VIEW)



logic diagrams (positive logic)



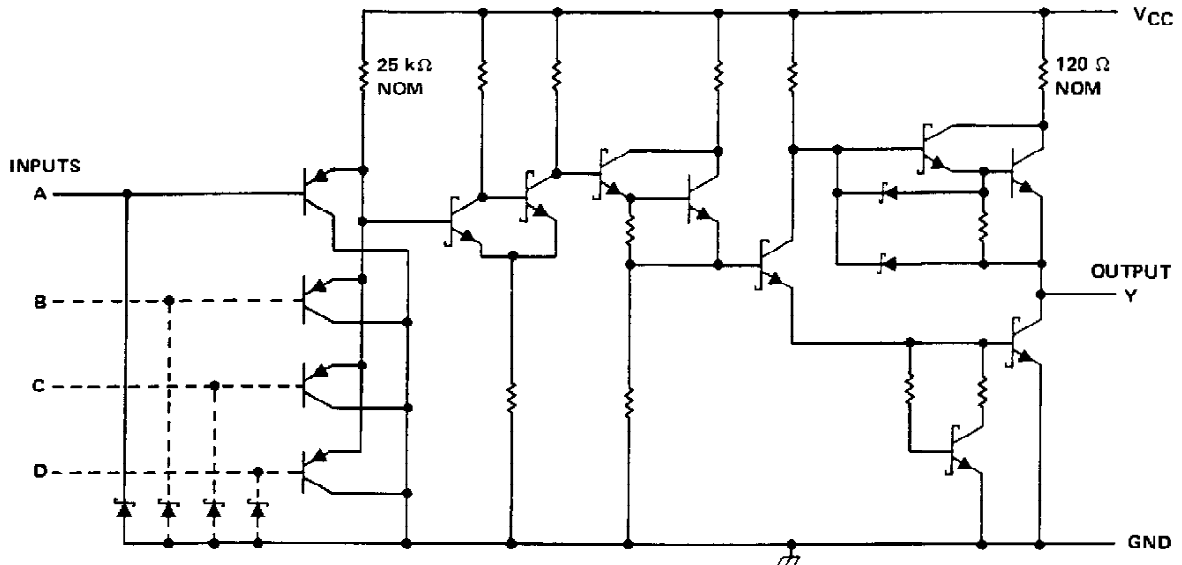
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN74LS19A, SN74LS24A
SCHMITT-TRIGGER POSITIVE-NAND GATES
AND INVERTERS WITH TOTEM-POLE OUTPUTS

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-400	μ A
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

SN74LS19A, SN74LS24A
SCHMITT-TRIGGER POSITIVE-NAND GATES
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN TYP‡ MAX			UNIT	
		MIN	TYP‡	MAX		
V_{T+}	$V_{CC} = 5\text{ V}$	1.65	1.9	2.15	V	
V_{T-}	$V_{CC} = 5\text{ V}$	0.75	1.0	1.25	V	
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.9		V	
V_{IK}	$V_{CC} = \text{MIN.}$ $I_I = -18\text{ mA}$		-1.5		V	
V_{OH}	$V_{CC} = \text{MIN.}$ $V_I = V_{T-\text{min}}$ $I_{OH} = -0.4\text{ mA}$	2.7	3.4		V	
V_{OL}	$V_{CC} = \text{MIN.}$ $V_I = V_{T+\text{max}}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V	
		$I_{OL} = 8\text{ mA}$	0.35	0.5		
I_{T+}	$V_{CC} = 5\text{ V.}$ $V_I = V_{T+}$		-2	-20	μA	
I_{T-}	$V_{CC} = 5\text{ V.}$ $V_I = V_{T-}$		-5	-30	μA	
I_I	$V_{CC} = \text{MAX.}$ $V_I = 7\text{ V}$		0.1		mA	
I_{IH}	$V_{CC} = \text{MAX.}$ $V_I = 2.7\text{ V}$			20	μA	
I_{IL}	$V_{CC} = \text{MAX.}$ $V_I = 0.4\text{ V}$			-50	μA	
I_{OS}^{\S}	$V_{CC} = \text{MAX.}$ $V_I = V_O = 0\text{ V}$		-20	-100	mA	
I_{CCH}	$V_{CC} = \text{MAX.}$ $V_I = 0\text{ V}$	'LS19A		9.9	18	mA
		'LS24A		6.6	12	
I_{CCL}	$V_{CC} = \text{MAX.}$ $V_I = 4.5\text{ V}$	'LS19A		17	30	mA
		'LS24A		11	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V.}$ $T_A = 25^\circ\text{C.}$

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V,}$ $T_A = 25^\circ\text{C}$ (see Figure 1)

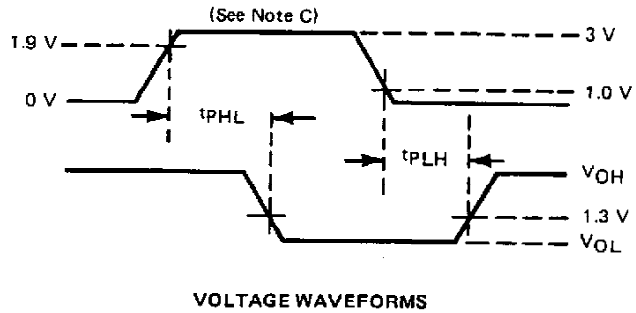
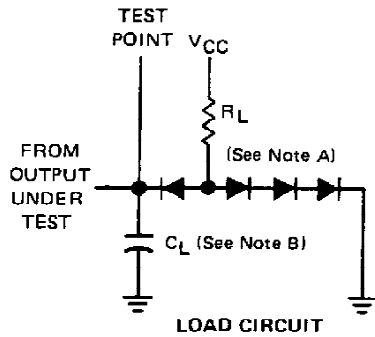
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74LS19A			SN74LS24A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	$R_L = 2\text{ k}\Omega,$ $C_L = 15\text{ pF}$		13	20		13	20	ns
t_{PHL}	Any	Y			18	30		25	40	ns

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All diodes are IN3064 or equivalent.
 B. C_L includes probe and circuit capacitance.
 C. The generator characteristics are: PRR = 1 MHz, $t_r = 15$ ns, $t_p = 6$ ns, $Z_o = 50 \Omega$.

FIGURE 1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS19ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS19ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS19ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS19ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS24AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74LS24AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS19ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS19ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS19ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LS19ANSR	SO	NS	14	2000	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

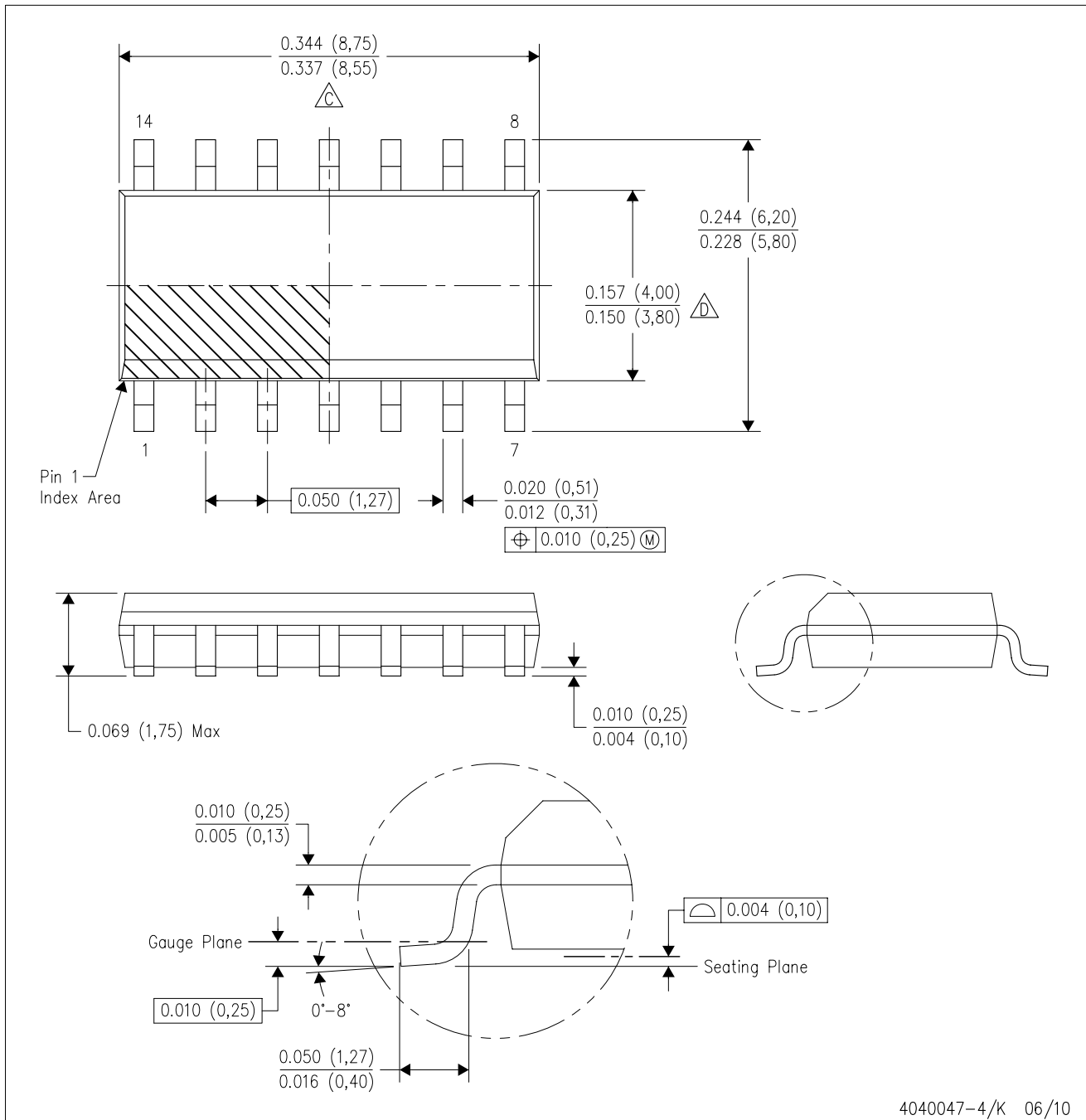
16 PINS SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

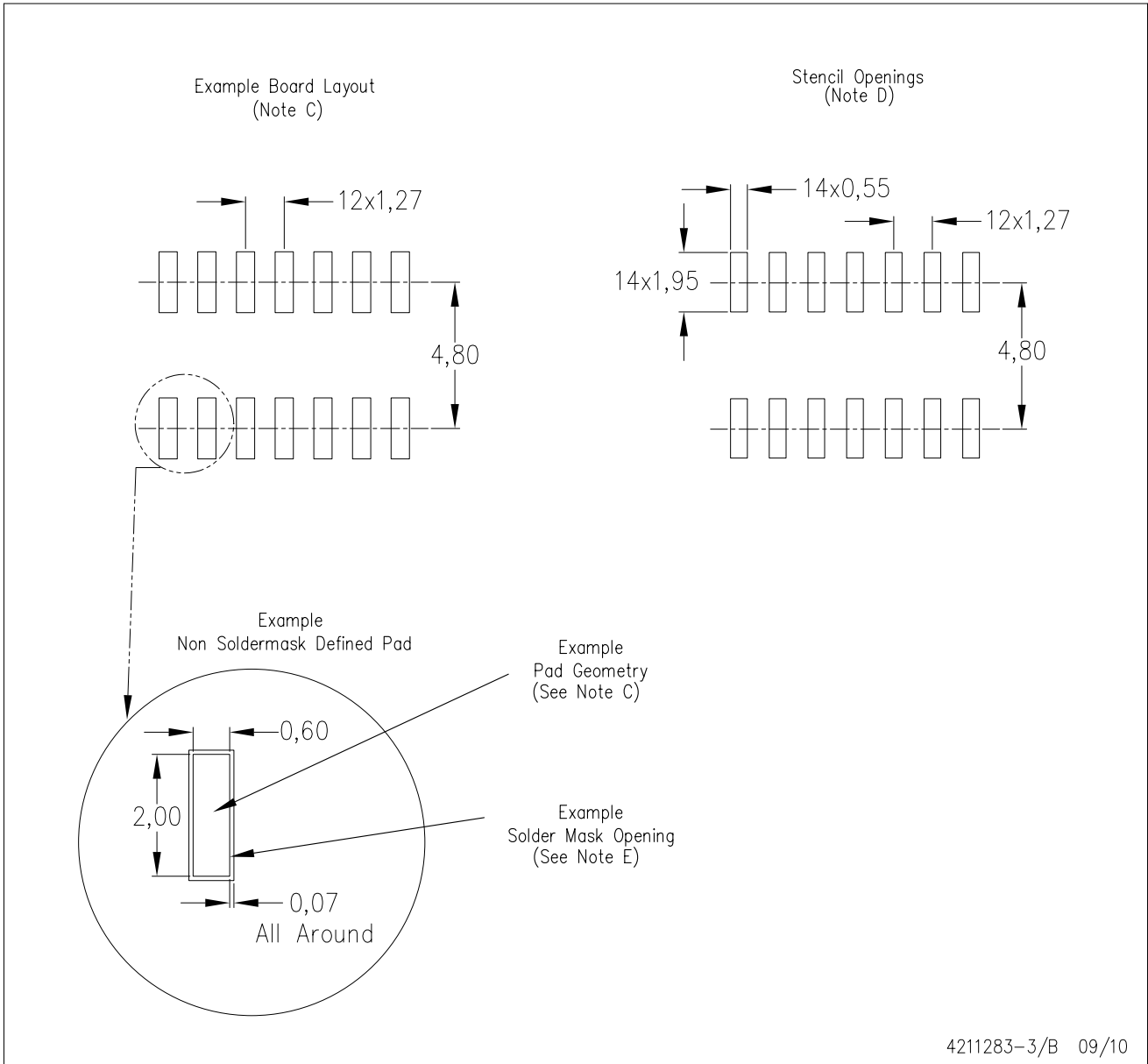
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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