

# SN74CBTS6800

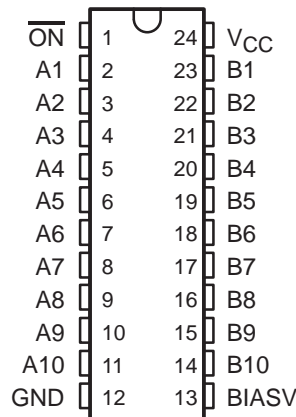
## 10-BIT FET BUS SWITCH

### WITH PRECHARGED OUTPUTS AND SCHOTTKY DIODE CLAMPING

SCDS102C – JUNE 1999 – REVISED OCTOBER 2000

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Schottky Diodes on the I/Os to Clamp Undershoots up to -2 V

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



#### description

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoots.

The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBTS6800 is organized as one 10-bit switch with a single enable ( $\overline{ON}$ ) input. When  $\overline{ON}$  is low, the switch is on, and port A is connected to port B. When  $\overline{ON}$  is high, the switch between port A and port B is open. When  $\overline{ON}$  is high or V<sub>CC</sub> is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	SOIC – DW	Tube	SN74CBTS6800DW	
		Tape and reel	SN74CBTS6800DWR	
	SSOP – DB	Tape and reel	SN74CBTS6800DBR	CS6800
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTS6800DBQR	CBTS6800
	TSSOP – PW	Tape and reel	SN74CBTS6800PWR	CS6800
	TVSOP – DGV	Tape and reel	SN74CBTS6800DGVR	CS6800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge



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**TEXAS  
INSTRUMENTS**

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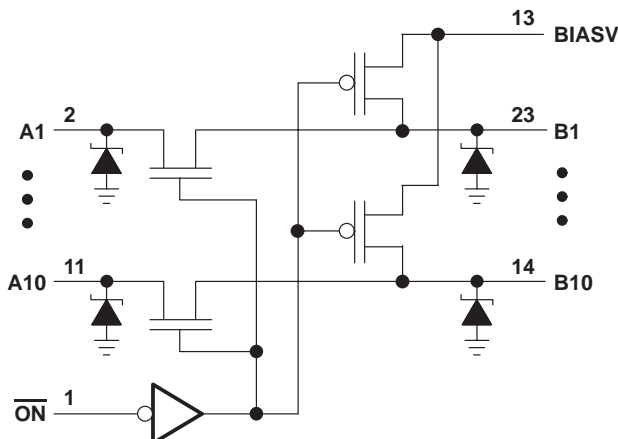
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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Bias voltage range, BIASV	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Continuous channel current	.....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):		
DB package	.....	63°C/W
DBQ package	.....	61°C/W
DGV package	.....	86°C/W
DW package	.....	46°C/W
PW package	.....	88°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	$V_{CC}$	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SCDS102C – JUNE 1999 – REVISED OCTOBER 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	A or B inputs	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-0.7	V
	Control inputs					-1.2	
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = GND			-5	μA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V			150	μA
I <sub>O</sub>		V <sub>CC</sub> = 4.5 V,	BIASV = 2.4 V, V <sub>O</sub> = 0	0.25			mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			3	μA
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0			3.5		pF
C <sub>io</sub> (OFF)		V <sub>O</sub> = 3 V or 0,	$\overline{\text{ON}} = V_{CC}$		4.5		pF
r <sub>on</sub> §	V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V	V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		11	20	Ω
	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA	3	7		
			I <sub>I</sub> = 30 mA	3	7		
		V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA	6	15		

† All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

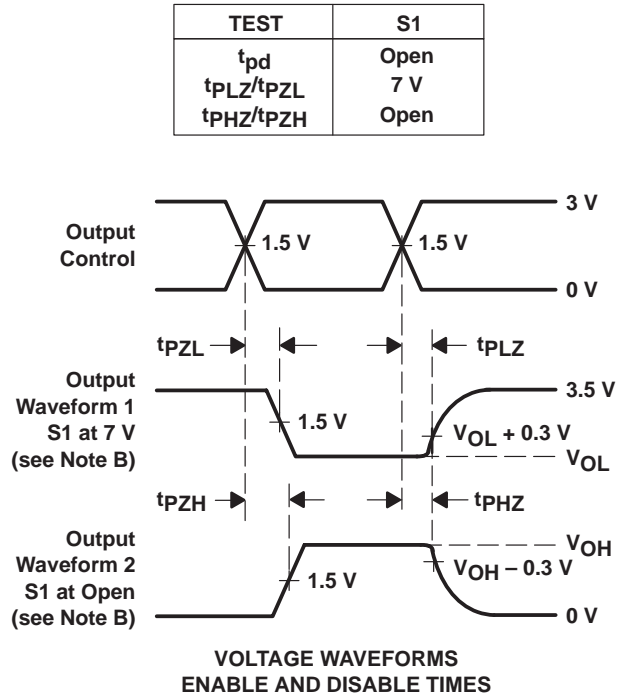
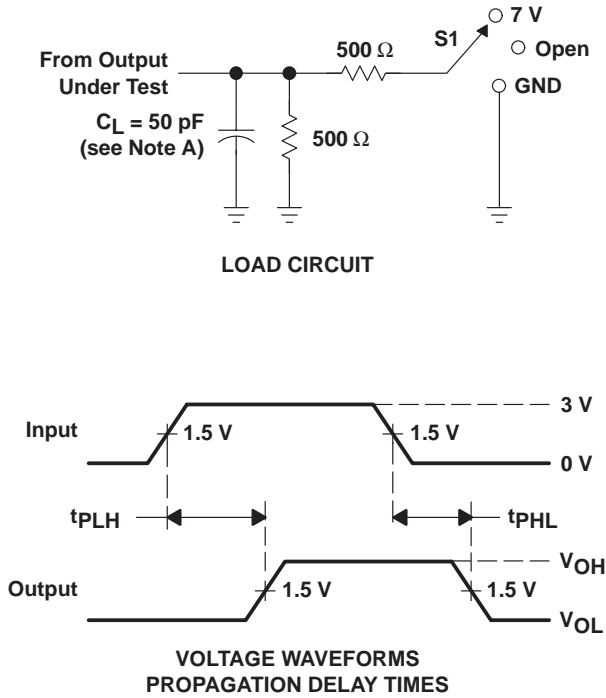
**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A			0.35		0.25	ns
t <sub>PZH</sub>	$\overline{\text{ON}}$	A or B	BIASV = GND		6	2	5.1	ns
t <sub>PZL</sub>			BIASV = 3 V		6	2	5.6	
t <sub>PHZ</sub>	$\overline{\text{ON}}$	A or B	BIASV = GND		5.5	1	5	ns
t <sub>PLZ</sub>			BIASV = 3 V		5.5	2	5.9	

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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 SCDS102C – JUNE 1999 – REVISED OCTOBER 2000

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. t<sub>PZL</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.  
 G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBTS6800DBQRE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTS6800DBQRG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTS6800DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTS6800DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DBQR	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CBTS6800DGV	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTS6800PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTS6800DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTS6800DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTS6800DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTS6800PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTS6800DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
SN74CBTS6800DGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
SN74CBTS6800DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74CBTS6800PWR	TSSOP	PW	24	2000	346.0	346.0	33.0



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

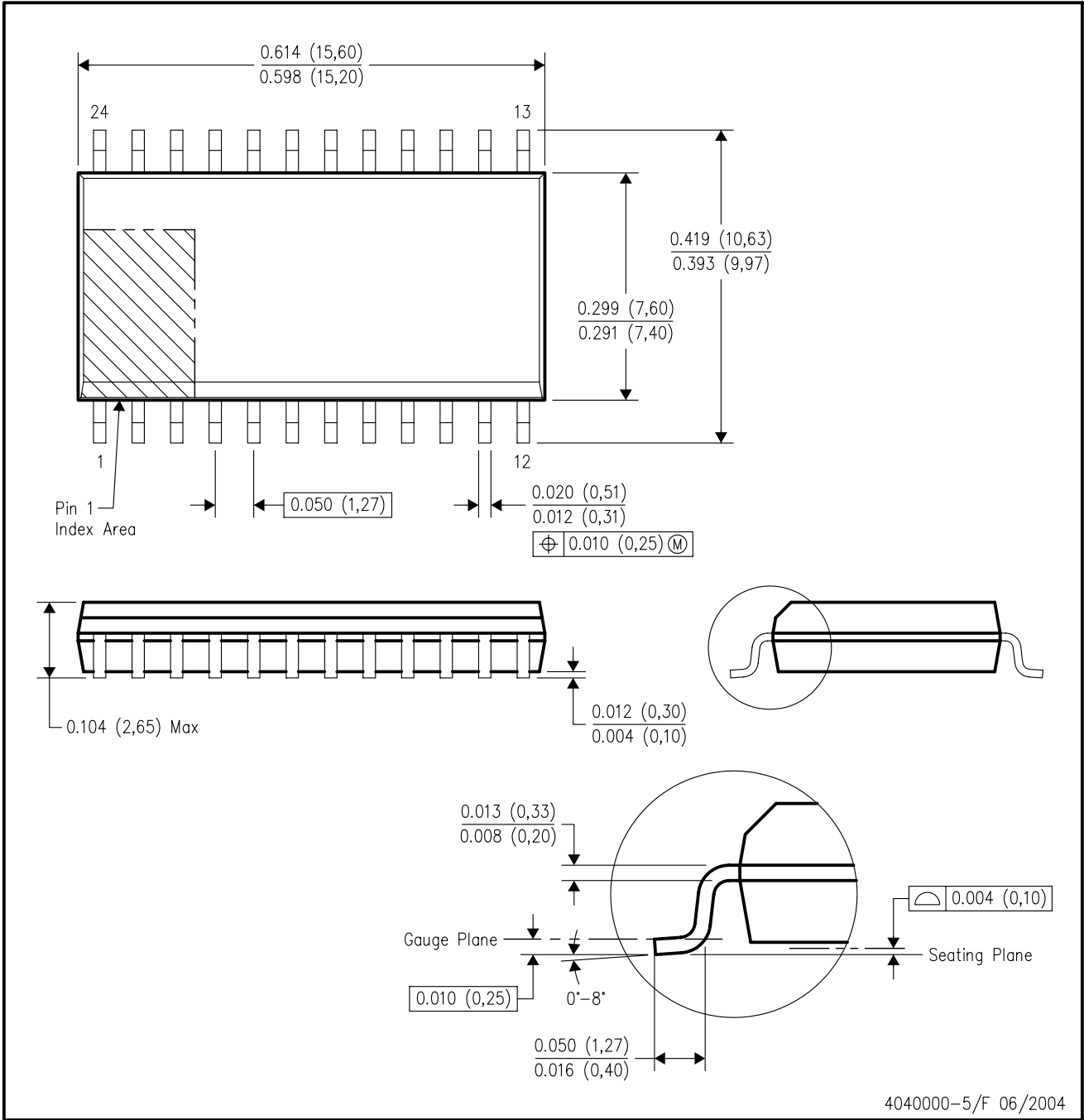


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- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

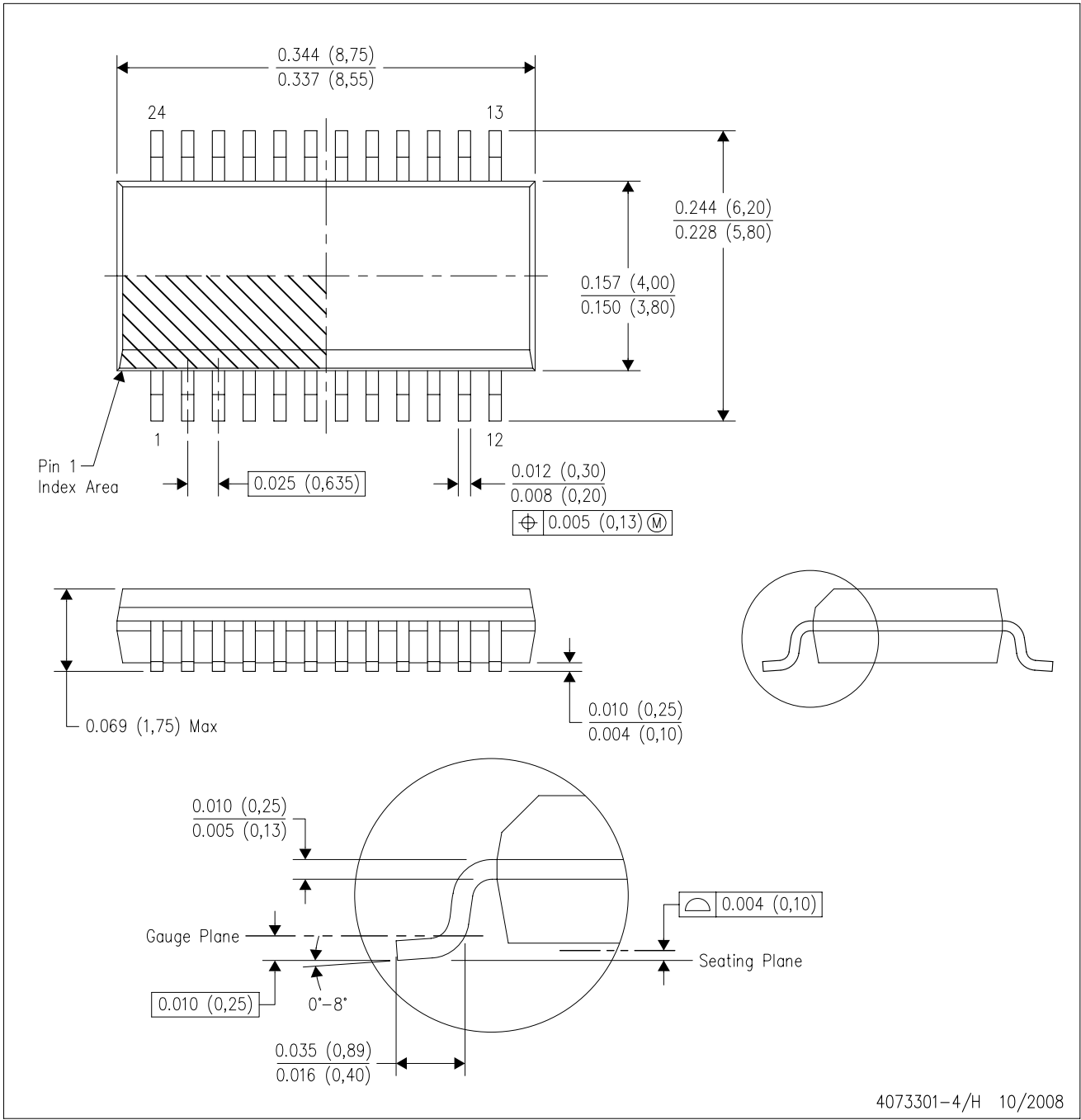
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

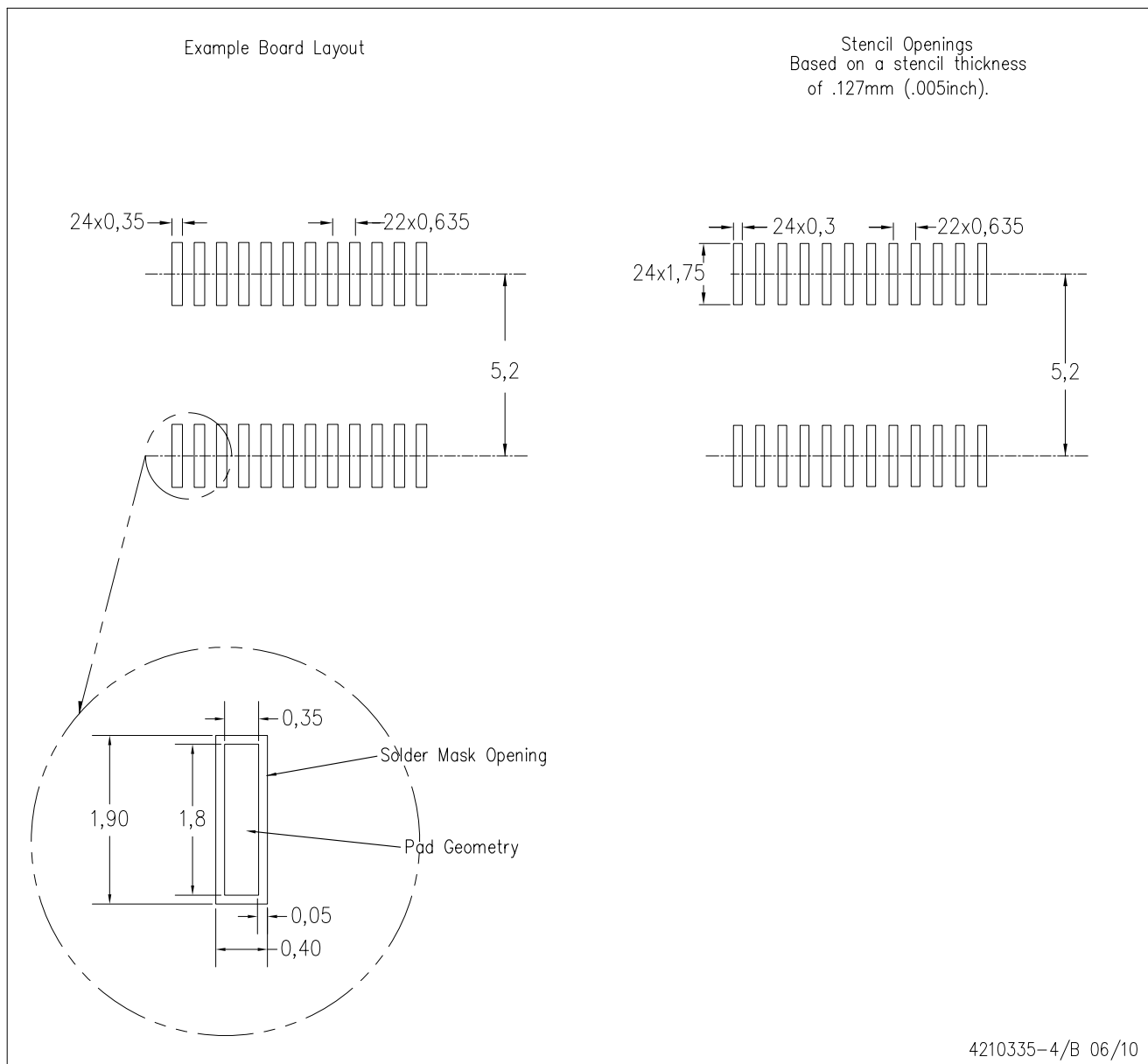
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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