Si590/591

1 ps MAX JITTER CRYSTAL OSCILLATOR (XO) (10 MHz TO 525 MHz)

Features

- Available with any-frequency output frequencies from 10 to 525 MHz
- 3rd generation DSPLL® with superior jitter performance: 1 ps max jitter
- Better frequency stability than SAW-based oscillators
- Internal fundamental mode crystal ensures high reliability
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant
- –40 to +85 ºC operating temperature range

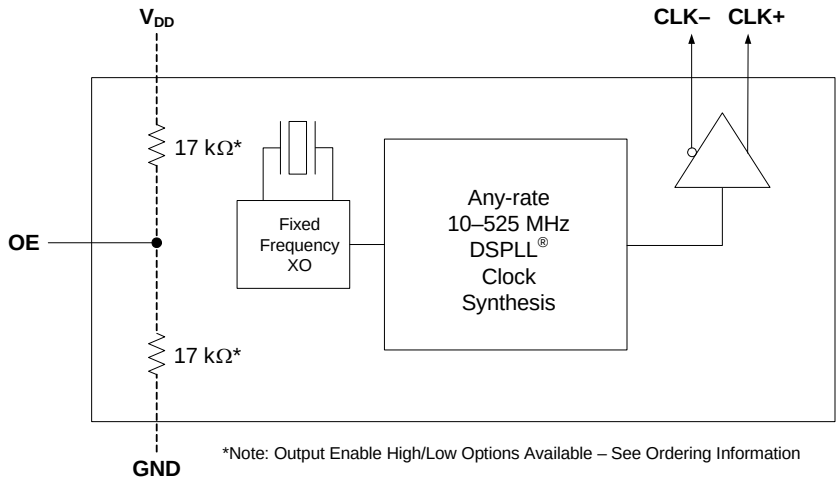
Applications

- SONET/SDH (OC-3/12/48)
- Networking
- SD/HD SDI/3G SDI video
- Test and measurement
- Storage
- FPGA/ASIC clock generation

Description

The Si590/591 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low jitter clock at high frequencies. The Si590/591 supports any frequency from 10 to 525 MHz. Unlike a traditional XO, where a unique crystal is required for each output frequency, the Si590/591 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si590/591 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, and stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

Functional Block Diagram



*Note: Output Enable High/Low Options Available – See Ordering Information

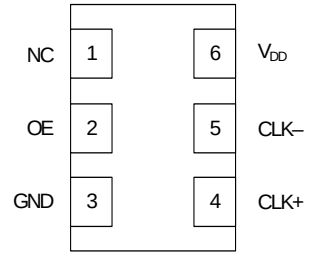
Ordering Information:

See page 6.

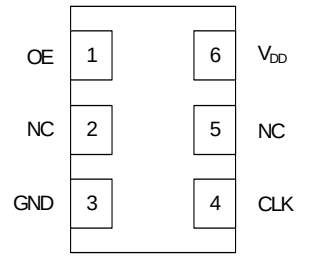
Pin Assignments:

See page 5.

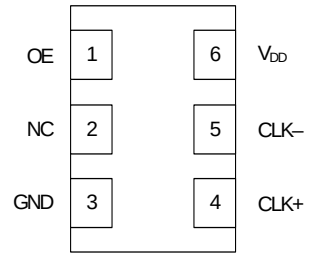
(Top View)



Si590 (LVDS/LVPECL/CML)



Si590 (CMOS)



Si591 (LVDS/LVPECL/CML)

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	Output enabled				mA
		LVPECL	—	110	125	
		CML	—	100	110	
		LVDS	—	90	100	
		CMOS	—	80	90	
		Tristate mode	—	60	75	
Output Enable (OE)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 6 for further details.
2. OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pull-down resistor to GND for output enable active low. See 3. "Ordering Information" on page 6.

Table 2. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency[1,2]	f_O	LVPECL/LVDS/CML	10	—	525	MHz
		CMOS	10	—	160	
Initial Accuracy	f_i	Measured at +25 °C at time of shipping	—	±1.5	—	ppm
Total Stability		Note 3, second option code “C”	—	—	±30	ppm
		Note 4, second option code “B”	—	—	±50	ppm
		Note 4, second option code “A”	—	—	±100	ppm
Temperature Stability		second option code “C”	—	—	±20	ppm
		second option code “B”	—	—	±25	ppm
		second option code “A”	—	—	±50	ppm
Powerup Time[5]	t_{OSC}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 6 for further details.
2. Specified at time of order by part number.
3. Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 10 years aging at 40 °C. See 3. "Ordering Information" on page 6.
4. Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 15 years aging at 70 °C. See 3. "Ordering Information" on page 6.
5. Time from powerup or tristate mode to f_O.

Table 3. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	mid-level	—	V_{DD} – 0.75	—	V
	V_{OD}	swing (diff)	0.70	0.95	1.20	V_{PP}
CMOS Output Option[3]	V_{OH}		0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}		—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF. Sinking or sourcing 12 mA for V_{DD} = 3.3 V, 6 mA for V_{DD} = 2.5 V, 3 mA for V_{DD} = 1.8 V.

Table 4. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1] for 50 MHz ≤ F_{OUT} ≤ 525 MHz (LVPECL/LVDS/CML)	ϕ_J	12 kHz to 20 MHz	—	0.5	1.0	ps
Phase Jitter (RMS)[1] (LVPECL/LVDS/CML)	ϕ_J	12 kHz to 20 MHz, 155.52 MHz output frequency	—	0.4	0.69	ps
Phase Jitter (RMS)[2] for 50 MHz ≤ F_{OUT} ≤ 160 MHz (CMOS)	ϕ_J	12 kHz to 20 MHz	—	0.6	1.0	ps

Notes:
1. Differential Modes LVPECL/LVDS/CML. 3.3 and 2.5 V supply voltage options only.
2. Single-ended CMOS output phase jitter measured using 33 Ω series termination into 50 Ω phase noise test equipment. 3.3 V supply voltage option only.

Table 5. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	—	3	ps
		Peak-to-Peak	—	—	35	
***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.						

Table 6. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	ºC
Supply Voltage, 1.8 V Option	V_{DD}	–0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	Volts
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

Table 7. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

2. Pin Descriptions

(Top View)

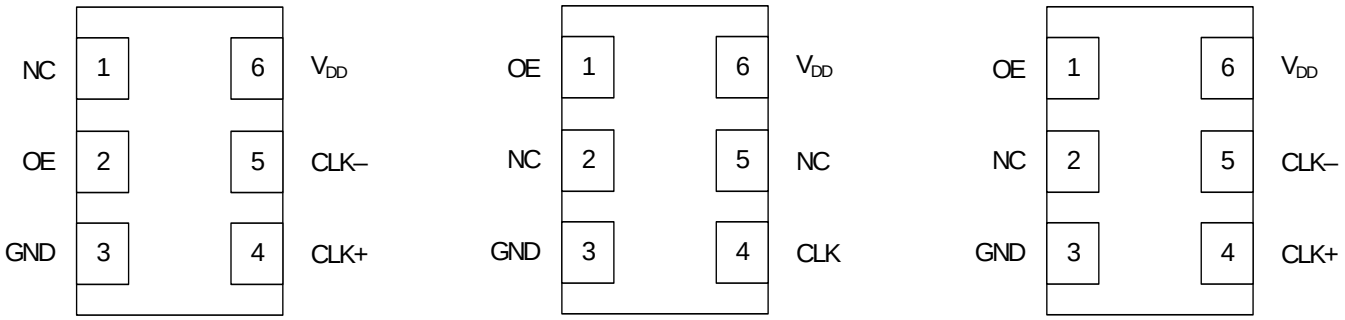


Table 8. Pinout for Si590 Series

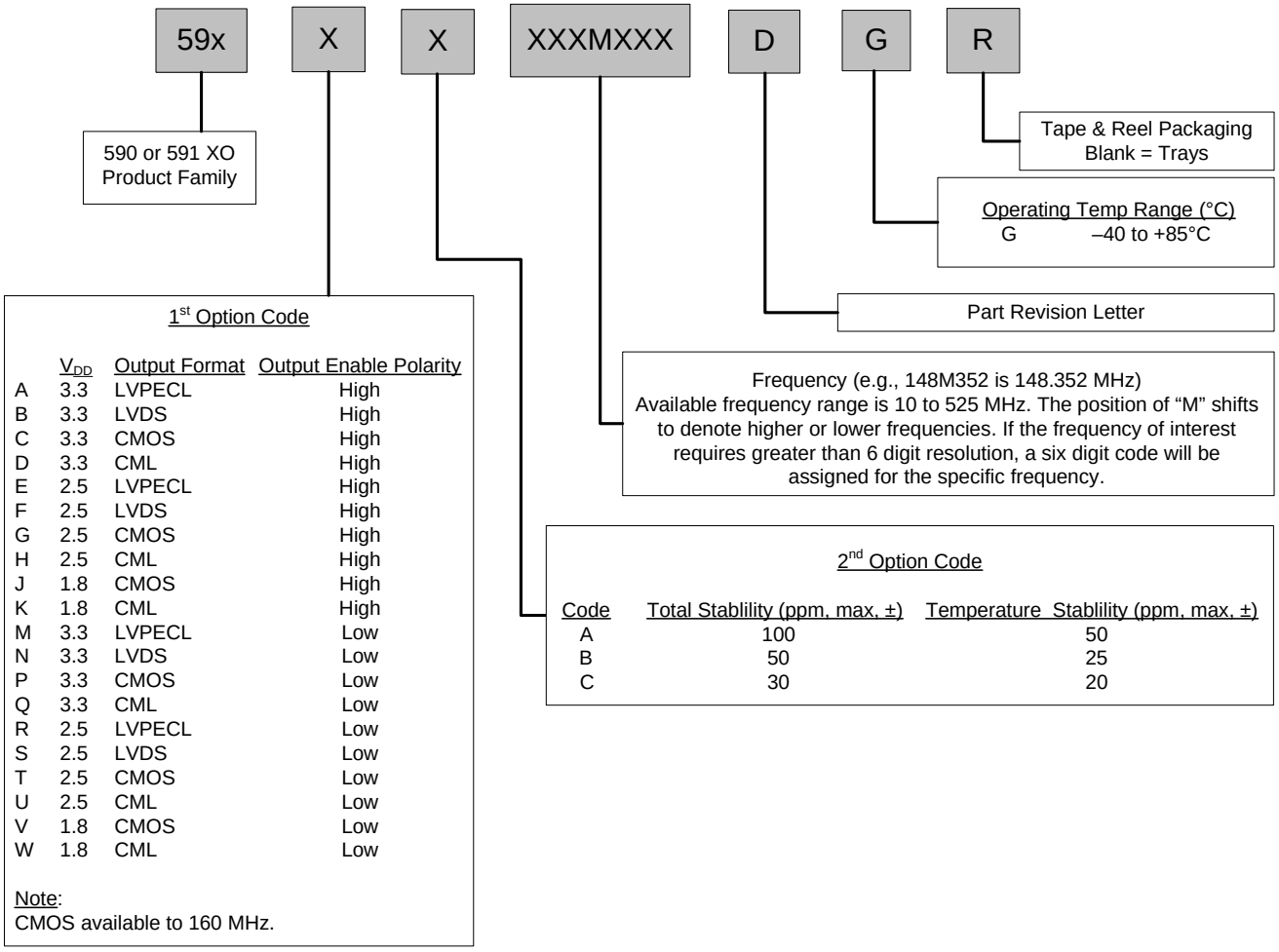
Pin	Symbol	LVDS/LVPECL/CML Function	CMOS Function
1	OE*	No connection Make no external connection to this pin	Output enable
2	OE*	Output enable	No connection Make no external connection to this pin
3	GND	Electrical and Case Ground	Electrical and Case Ground
4	CLK+	Oscillator Output	Oscillator Output
5	CLK–	Complementary Output	No connection Make no external connection to this pin
6	V_{DD}	Power Supply Voltage	Power Supply Voltage
***Note:** OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 6.			

Table 9. Pinout for Si591 Series

Pin	Symbol	LVDS/LVPECL/CML Function
1	OE*	Output enable
2	No connection Make no external connection to this pin	No connection Make no external connection to this pin
3	GND	Electrical and Case Ground
4	CLK+	Oscillator Output
5	CLK–	Complementary output
6	V_{DD}	Power Supply Voltage
***Note:** OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 6.		

3. Ordering Information

The Si590/591 XO supports a variety of options including frequency, temperature stability, output format, and V_{DD}. Specific device configurations are programmed into the Si590/591 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si590 and Si591 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The Si591 Series supports an alternate OE pinout (pin #1) for LVPECL, LVDS, and CML output formats. See Tables 8 and 9 for the pinout differences between the Si590 and Si591 series.



Example P/N: 590BB148M352DGR is a 5 x 7 XO in a 6 pad package. The frequency is 148.352 MHz, with a 3.3 V supply, LVDS output, and Output Enable active high polarity. Overall stability is specifed as ±50 ppm. The device is specified for –40 to +85 °C ambient temperature range operation and is shipped in tape and reel format.

Figure 1. Part Number Convention

4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si590/591. Table 10 lists the values for the dimensions shown in the illustration.

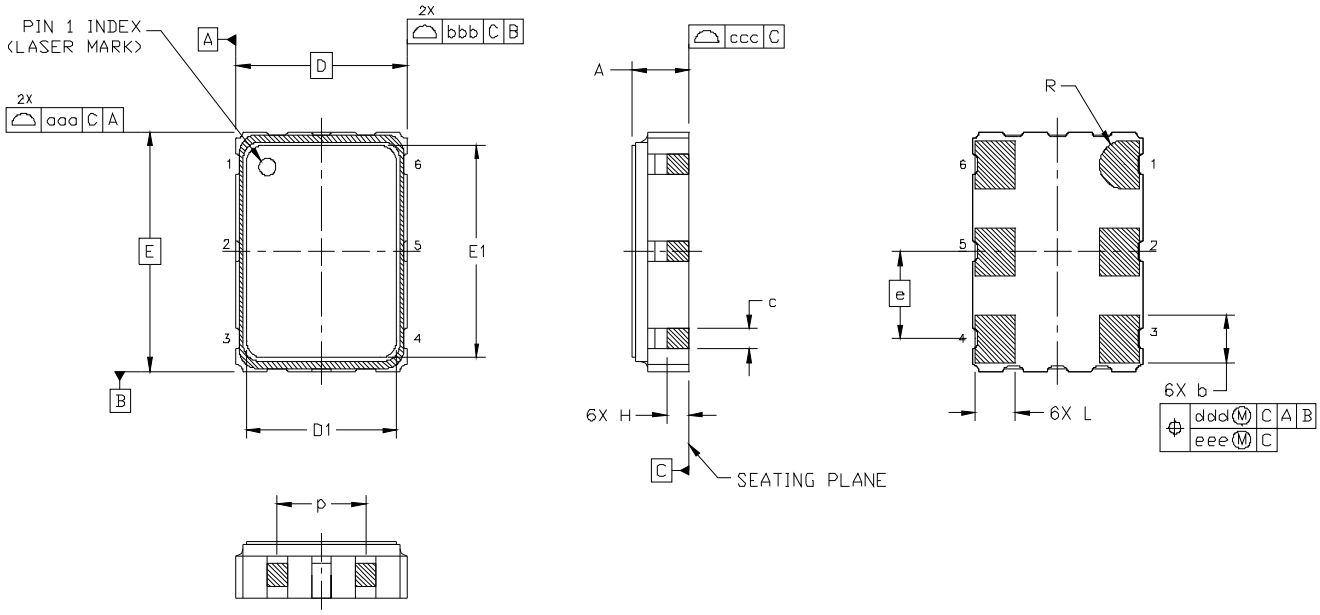


Figure 2. Si590/591 Outline Diagram

Table 10. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
p	1.80	—	2.60
R		0.70 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.50	

5. Si590/Si591 Mark Specification

Figure 3 illustrates the mark specification for the Si590/Si591. Table 11 lists the line information.

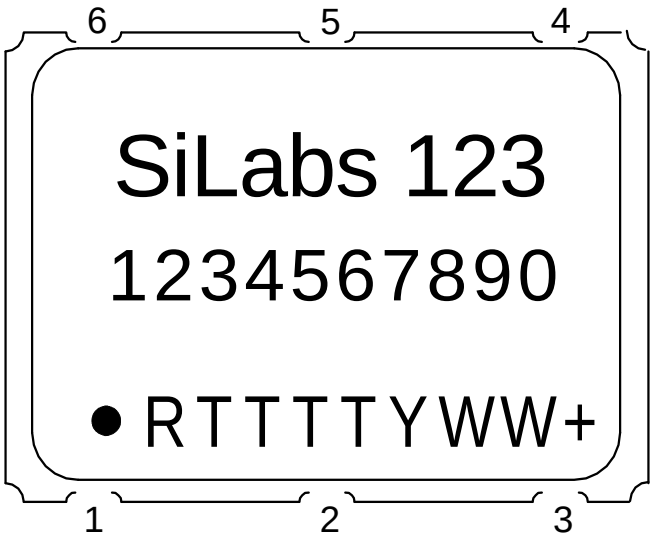


Figure 3. Mark Specification

Table 11. Si53x Top Mark Description

Line	Position	Description
1	1–10	"SiLabs"+ Part Family Number, 59x (First 3 characters in part number)
2	1–10	Si590, Si591: Option1 + Option2 + Freq(7) + Temp Si590/Si591 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	"+" to indicate Pb-Free and RoHS-compliant

6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si590/591. Table 12 lists the values for the dimensions shown in the illustration.

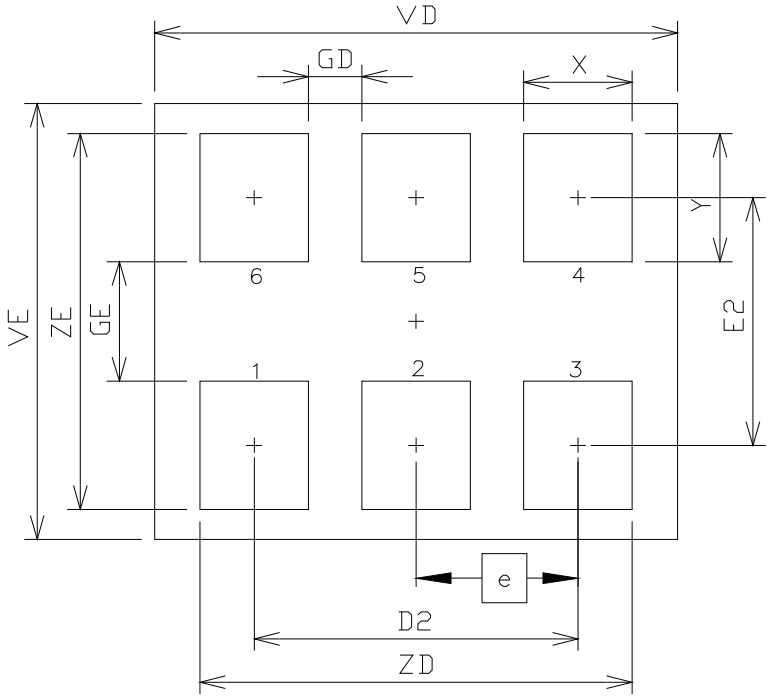


Figure 4. Si590/591 PCB Land Pattern

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Table 12. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.25

- Total Stability Maximum changed to ±30 in Table 2 on page 2.
- Total Stability Maximum changed to ±30 in Figure 1 on page 6.

Revision 0.25 to Revision 0.3

- Updated Table 4 on page 3 by adding the 155.51 MHz “Phase Jitter (RMS) (LVPECL/LVDS/CML)” row.
- Updated and clarified Table 7 on page 4 to correct typos and include the “Moisture Sensitivity Level” and “Contact Pads” rows.
- Corrected BSC value in rows D and E in Table 10 on page 7.

NOTES:

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